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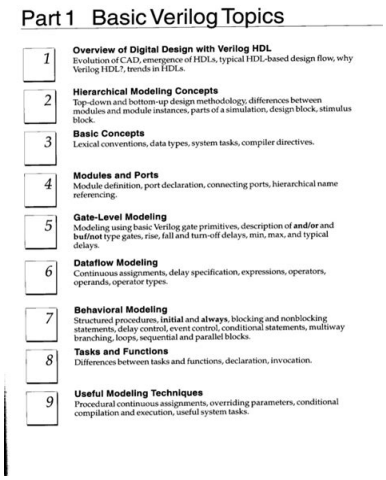
so many fake sites. this is the first one which worked! Many thanks



Part 1 Basic Verilog Topics

1 **Overview of Digital Design with Verilog HDL**
Evolution of CAD, emergence of HDLs, typical HDL-based design flow, why Verilog HDL?, trends in HDLs.

2 **Hierarchical Modeling Concepts**
Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.

3 **Basic Concepts**
Lexical conventions, data types, system tasks, compiler directives.

4 **Modules and Ports**
Module definition, port declaration, connecting ports, hierarchical name referencing.

5 **Gate-Level Modeling**
Modeling using basic Verilog gate primitives, description of **and/or** and **buf/not** type gates, rise, fall and turn-off delays, min, max, and typical delays.

6 **Dataflow Modeling**
Continuous assignments, delay specification, expressions, operators, operands, operator types.

7 **Behavioral Modeling**
Structured procedures, **initial** and **always**, blocking and nonblocking statements, delay control, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.

8 **Tasks and Functions**
Differences between tasks and functions, declaration, invocation.

9 **Useful Modeling Techniques**
Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

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